SURFACE FINISHING

FOR

PRINTED CIRCUIT BOARDS

In a world of ever-increasing electronic component complexity and pin count requirements for component packaging, focus is once again on the age-old question of "How do we preserve solderable surfaces between PWB manufacturing and assembly?" PCB manufacturers today are faced with the decision of which surface finish to offer their customers, while their customers struggle with choosing the best surface coating for their application. Ultimately, the surface coating choice belongs to the end user, or customer, not the PCB manufacturer. This article will discuss the various surface coatings and characteristics of each.

The variables that must be considered when choosing the best surface finish are too numerous to list here. The following are the most common process variables of concern at assembly:

- Component type and placement method
- Solder paste type and application (if applicable)
- Fusing method
- Possible exposure of each board type to a variety of assembly processes
- Multiple thermal exposures
- Post cleaning (if applicable)

Less common considerations include the elimination of CFCs and the possible exclusion of leaded solders, solder paste, and flux at assembly.
Choices for solderable finishes include organic solderability preservatives (OSPs), immersion, electrolytic and electroless nickel/gold, and fused or hot air leveled solder. Solder has traditionally been the preferred coating.

OSPs are available in many forms and would clearly be the finish of choice if the decision were the sole responsibility of the PCB manufacturer. The application of an organic surface finish is easy to apply and cost effective. It also eliminates the need for lead-bearing solders in one PCB manufacturing process. OSPs may work well in some assembly processes that do not require extended shelf life prior to assembly and are not exposed to multiple fusing cycles. It is generally agreed that OSP coatings require special handling to retain solderability over a period of time.

However, there are several concerning issues involved with the use of OSPs. When using an organic coating, the solderability of the PCB is not proven until the assembly process. Surface contaminites such as tin left behind in the solder or tin stripping process, copper oxides, soldermask residues, and even clean copper surfaces brightened with excessive organic plating additives can leave a PCB unsolderable. OSPs can be applied over any of these conditions which will not be highlighted until the board fails at assembly. At this stage, rework is very costly since components are now involved.

No-clean fluxes, which should be dominant in the near future, present another potential problem for the OSPs. They are often incompatible with no-clean fluxes. In many cases, these fluxes are not capable of penetrating the organic surface to activate and create a solderable condition. OSP coatings are designed to be a barrier to corrosion and copper oxide. They are removed or broken down by acids and heat. Low acid aqueous-based no-clean fluxes are what typical OSPs are designed to repel. There are many issues that present themselves when OSP coatings are used with the new, less aggressive no-clean fluxes. These obstacles emerge in many forms, from exposed copper to insufficient solder wetting and hole fill (Reference Figure 1). The new formulations that indicate better wetting results are very expensive and have very tight process windows within which PH levels must be kept.

The thickness of the coating can also have a negative effect on the board's ability to be electrically tested. If the coating is too thick, it can interfere with the continuity between a test probe and the point being tested.

OSPs are being used in several applications with varying degrees of success. It is interesting that age-old criteria for PCB reliability has been altered for OSP acceptability. Shelf life, coverage and through-hole fill are just a few of these changes. Evaluations have shown exposed copper and incomplete hole fill at wave solder. These have been explained away as insignificant even if such defects are cause for
rejection on a HAL-soldered PCB. The conclusions of these evaluations state that OSPs are acceptable for the application, and there is no significant difference when compared to other coatings (Reference Figures 1, 2, and 6).

A nickel/gold finish offers solutions to some of the shortcomings of the OSPs. Electrical test is not impaired by the presence of nickel/gold. The gold finish is easily activated by mild fluxes, which makes this finish more compatible with the no-clean fluxes. A nickel/gold finish is capable of withstanding numerous assembly operations with no degradation of the board's solderability. In spite of these advantages, like the OSPs, there are performance issues which limit the effectiveness of the nickel/gold finish.

First, gold is a contaminate of solder. While it is true that a "thin enough" coating of gold absorbed into a "thick enough" deposit of solder paste will probably not effect the quality of the solder joints, the process tolerances in both the gold and solder paste application process are allowed very little latitude. Gold concentrations below 0.5% in solder do not show any problems. The shear strength is slightly influenced by the gold at these concentrations and considered acceptable. It is recommended that the gold concentration be kept below 3.0wt% to prevent brittle and fractured joints. Gold-tin intermetallic formed on the surface of copper-rich alloys reduces the low fatigue life of the joints drastically. Gold concentrations over 4.0wt% result in many voids in the solder joint. Like the OSPs, electroless nickel/gold can be applied over a contaminated surface, which can cause solder joint failure. Electrolytic nickel/gold is an expensive process and generally time consuming. Electrolytic nickel with electroless gold is the more expensive nickel/gold process.

Both nickel/gold and OSPs cannot perform in assembly processes where the pre-soldered, HAL circuit board is required to carry the full volume of solder necessary to make the solder joint, such as hot bar soldering and some TAB assembly processes. Nickel/gold does work well with the more expensive wire bonding process.

Both nickel/gold and OSPs require the same bond to occur at assembly. This allows the solder paste to melt and sizzle prior to pad wetting. The time required to wet a solder joint allows for increased solder ball production at solder temperature.

Solder is, and always will be, the best finish to use when fusing to solder paste or to itself. Solder has the shortest wetting times at assembly and requires the least amount of activation from assembly fluxes, which makes it the most compatible with no-clean assembly processes. When evaluating HAL capability, it is useful to remember there is a difference between vertical and horizontal HAL.
The most globally used process is hot air solder leveling (HAL). For years, PWB component pads have been coated with solder using HAL. This coating provides excellent shelf life, high mechanical durability, and the shortest solder wetting time at assembly. It is also a fact that an intermetallic (IMC) bond is formed before the PWB assembly process, and maintains solderability through multiple reflow and wave soldering cycles (Reference Figure 6-8).

While the HAL process is affected by the same copper cleanliness issues as OSPs and nickel/gold, the effects are found in the PCB manufacturing process, not at assembly. The formation of the copper intermetallic at horizontal HAL assures that the PCB is solderable prior to shipping.

The HAL process has come under fire recently as assemblers, driven to finer pitch SMT devices, require "flatter" pads. It is alleged that the dome shape of HAL pads can present a serious challenge to the stencil printing operation used to deposit solder paste on the boards for assembly, especially in fine pitch applications.

The nature of the HAL process is to create a mound of solder on the SMD pads. The degree of unevenness of this mound, if excessive, can cause misalignment of SMT devices during assembly. Teledyne Electronic Technologies, Halco facility, has participated in several evaluations which have shown no indication of this dome shape presenting a real problem at assembly. The fine pitch tests we have been involved with have all indicated that the horizontal HAL provided a preferred solderable surface. The true requirement in assembly is not necessarily flat pads. The requirement is for uniform pads. Those knowledgeable in the HAL process know that the horizontal HAL process is capable of producing a very uniform finish on SMD pads on a printed circuit board. Thickness uniformity is typically well within a three sigma range from pad to pad within a feature group (Reference Figure 3).

There are two basic processes for HAL, vertical and horizontal. All reference to horizontal HAL is based on the Unicote® horizontal HAL process. Other horizontal processes may produce results inconsistent with data and capability referenced in this article.

One of the age-old concerns with HAL that is not present with OSPs or nickel/gold is thermal shock. Thermal shock is inevitable whenever the PWB is immersed in solder. However, the horizontal process minimizes the thermal stress on the panel by allowing a more gradual preheat and minimizes the dwell time in the solder to two (2) uniform seconds (Reference Figure 4). A major concern related to thermal stress is an increased warp and twist in the panel. The horizontal process affects the warp and twist no more than a typical oven bake according to testing (Reference IPC-TP-928).
There are basic process differences between the vertical and horizontal processes that have a major effect on the results. By the nature of the vertical process, the first or leading edge can see several seconds longer solder dwell time than the last or trailing edge. A copper-tin intermetallic compound (IMC) study in 1990 (Reference IPC-TP-928) shows that the average IMC thickness from the horizontal HAL, with a uniform two (2) second dwell time, is 6 microinches (0.152 micron), this compared to a one-pass vertical process with an average IMC thickness of 12.6 to 17.6 microinches (0.320 to 0.447 micron) (Reference Figure 9). While the IMC layer has to be present for solder to bond to the copper, an exposed IMC surface is not solderable. This makes IMC thickness very important to the solderability and shelf life of PWBs. With surface mount features becoming more and more complex, the minimum thickness most frequently specified range from 35 to 100 microinches. Vertical HAL has an IMC thickness that indicates solderability could be an issue in these ranges.

Perhaps the most critical difference in the capability between the vertical and horizontal process is that of thickness and uniformity. HAL is a geometrically dependent process. The nature of vertical HAL provides a challenge to control the natural sag or teardrop of solder which tends to form at the bottom of the pad or through-hole. Consequently, panels with QFP designs will typically have a bimotal thickness distribution on panels from vertical HAL. The north/south direction (top to bottom) will be considerably thinner than those in the east/west direction (right to left) (Reference Specification Guidelines for Hot Air Solder Leveling, Rev 3). This thickness difference is often enough to create solder paste problems at assembly and/or fail to meet customer required thickness specifications. It is not uncommon for a vertical processed panel with 25 mil pitch features to have a solder thickness range from 70 to 1500 microinches, with very high standard deviations. Sample data shows the thickness distribution and it is understandable that this could cause problems with component placement at assembly. Panels with features having this type of requirement at assembly should not be processed on vertical HAL equipment. Some vertical manufacturers have attempted to address this problem by using a clamping device that allows the panel to process at a 45° angle. While this helps, it only addresses one of the contributing control factors, and thickness ranges are still quite wide.

The horizontal HAL process allows the panel to be processed at an angle. The optimum angle for processing is 45°. This process provides a three sigma thickness range using a 70 microinch LCL and an 800 microinch UCL for the most critical features down to 20 mil pitch. Panels prevented from processing at a 45° angle due to physical restraints will still be processed at some angle and not straight. Although the QFP features processed at less than 45° angles will have a bimotal thickness distribution, studies indicate that most customer specification ranges can be achieved on panels with QFPs down to 25 mil pitch by processing with a minimum of a 29° angle. However, they will have a higher standard
deviation than panels processed at 45° angles but a tighter range and smaller deviation than the vertical process produces. Panels processed at a 29° angle typically cause no problems at assembly.

HAL is compatible with fine pitch technology products. The horizontal Unicote® Model 175 system produces product routinely down to 20 mil pitch. It operates effectively in a range of 70 to 800 microinches. Special thickness requirements have been met on request. Some TAB, 10 and 15 mil pitch panels have been processed with very good results. Process windows are tighter with ultra fine pitch product. The 45° angle becomes critical on this product. These panels are difficult to obtain and consequently more data is necessary. No defects at assembly were attributed to HAL in any of the studies we have participated in to date. However, there were component and placement issues that remain unresolved. Production information is to date thin, but these are certainly encouraging results and indicate HAL is capable of providing the entire volume of solder needed to assemble ultra fine pitch devices by hot bar or reflow methods (Reference Figure 10).

The introduction of lead-free alloys which are compatible with the HAL process eliminate concerns of potential health and environmental hazards caused by lead-bearing solders. It is fact that lead and lead containing solders are a perceived problem. Teledyne is addressing the issue and is presently collaborating with Aim Products in evaluating a lead-free alloy called Castin. Castin is thought to be compatible with SN63 solder which would make for an easy transition. PCB manufacturers could HAL with Castin and end users could assemble with SN63 during transition. Evaluations are in very early stages with preliminary data looking very promising. The Unicote® Model 175 horizontal HAL was used for testing and results are very similar to those of SN63 (see no-lead charts Figure 3,5,7, and 8).

Much work remains as technologies change. Certain applications may benefit from alternate surface finishes. However, solder is clearly the surface coating of choice for reliability, and continues to be the most widely used surface coating. With new technology eliminating the use of paste and active fluxes at assembly, thereby eliminating the need for post cleaning and having no residue remaining on the PCB, solder must be utilized from the pad itself. This technology certainly is not compatible with OSPs or nickel/gold coatings. It does, however, require continual evolution of horizontal HAL.

In conclusion, it is clear that each of the solderable finish options will work in certain production processes for specific assembly processes and acceptance standards. It is equally clear that the most versatile and universally accepted PCB solderable finish is HAL. The most robust HAL is horizontal, giving the assembler the widest assembly process choices available.
REFERENCES

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3. *Specification Guidelines for Hot Air Leveling, Rev 3*


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6. IPC-TP-996, "No Clean" Assembly Process/PCB Material Compatibility


9. Teledyne and Aim Collaboration, 1/94, *Hot Air Leveling with No-Lead Solder*